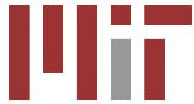


Positive-Bias Temperature Instability (PBTI) of GaN MOSFETs

Alex Guo and Jesús A. del Alamo

Microsystems Technology Laboratories (MTL)
Massachusetts Institute of Technology (MIT)
Cambridge, MA, USA

Sponsor: United States National Defense Science & Engineering Graduate Fellowship (NDSEG)

Purpose

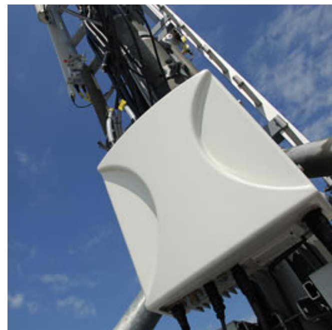
To understand the physics of and to mitigate PBTI in GaN n-MOSFETs.

Outline

1. Introduction
2. Experimental setup
3. PBTI results
4. Discussion and modeling
5. Conclusions

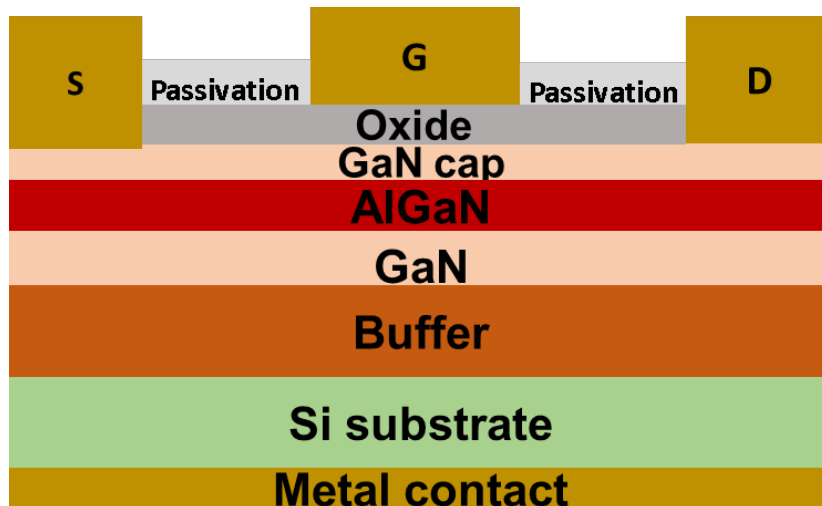
1. Introduction

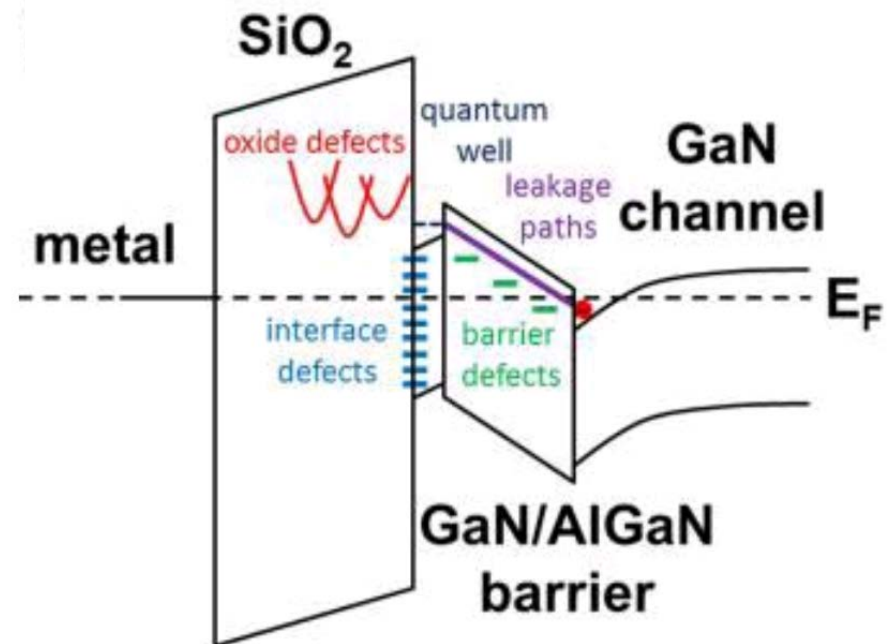
- GaN promising for power electronics
- Positive-Bias Temperature Instability (PBTI) is a concern:
    - Operational instability
    - Long-term reliability issue
- Challenge: mechanisms responsible for PBTI?



Favored structure: GaN MIS-HEMT

- MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor
- Why GaN MIS-HEMT: Large gate swing, low gate leakage



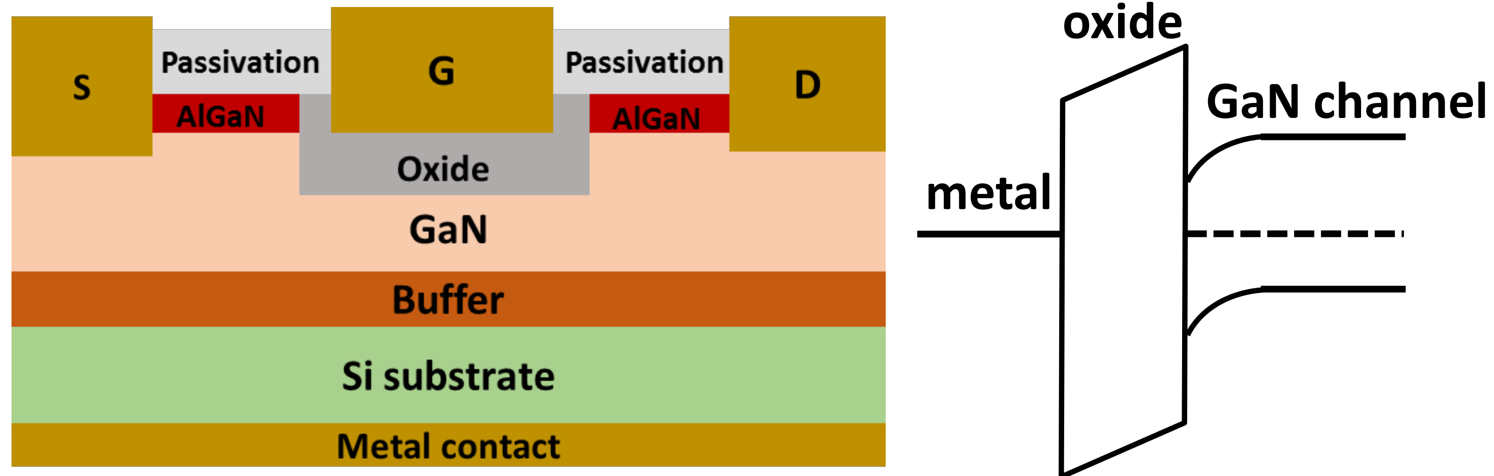


P. Lagger, TED 2014

- Many layers and interfaces complicate PBTI picture
- Many possible sites for trapping

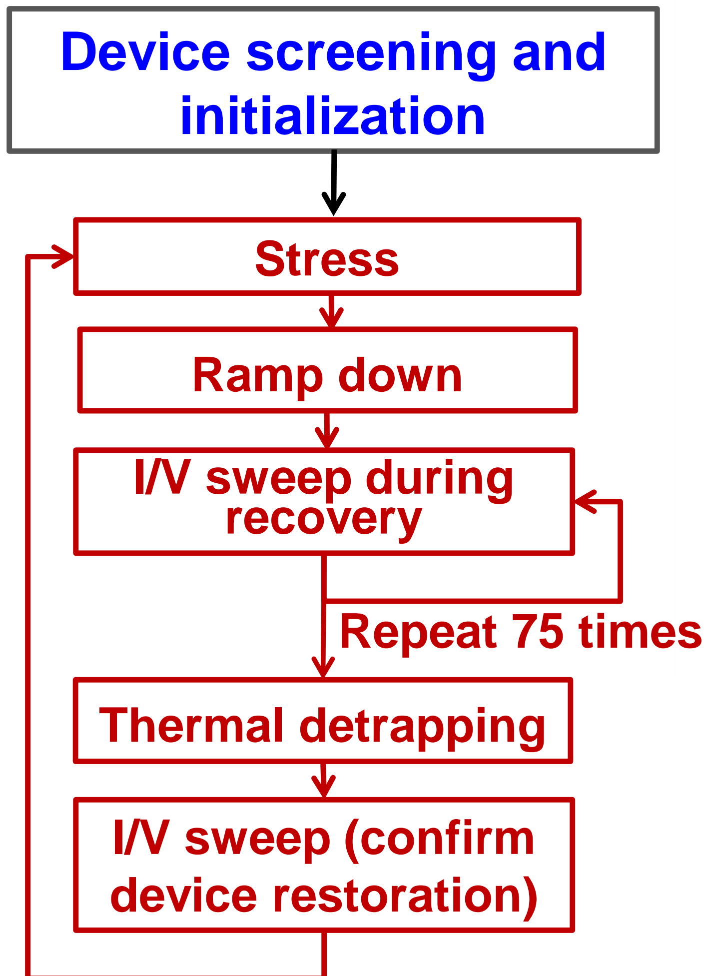
2. Experimental setup

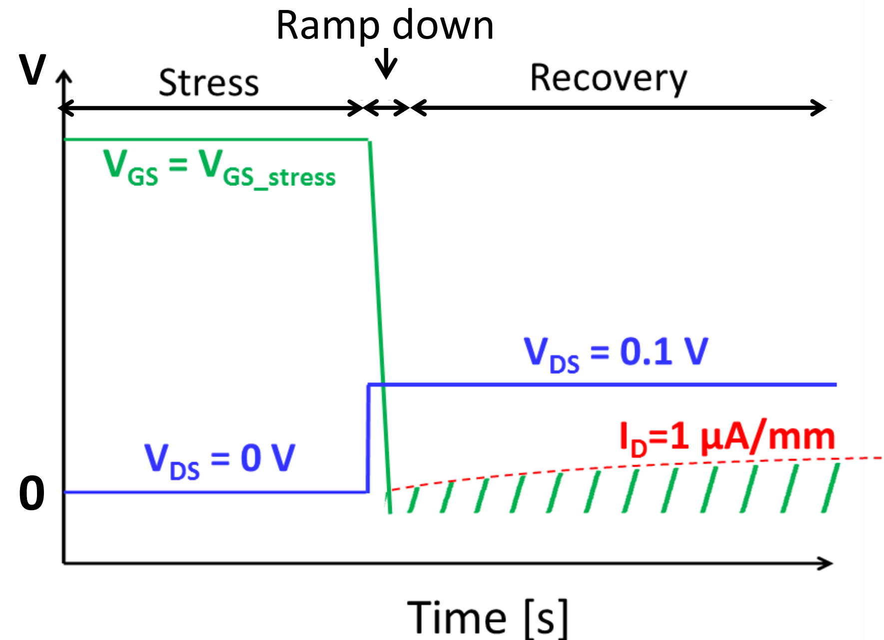
- **Simpler GaN MOSFET structure**



- **One interface: oxide/GaN interface**
- **Studied devices with two different gate dielectrics with same EOT:**
  - **SiO_2**
  - **SiO_2/Al_2O_3 composite**

PBTI experiment flow





- V_T : V_{GS} value when I_D = 1 μA/mm
- S : Extracted at I_D = 0.1 μA/mm
- g_{m_max}: Extracted on ramp down
- All at V_{DS} = 0.1 V

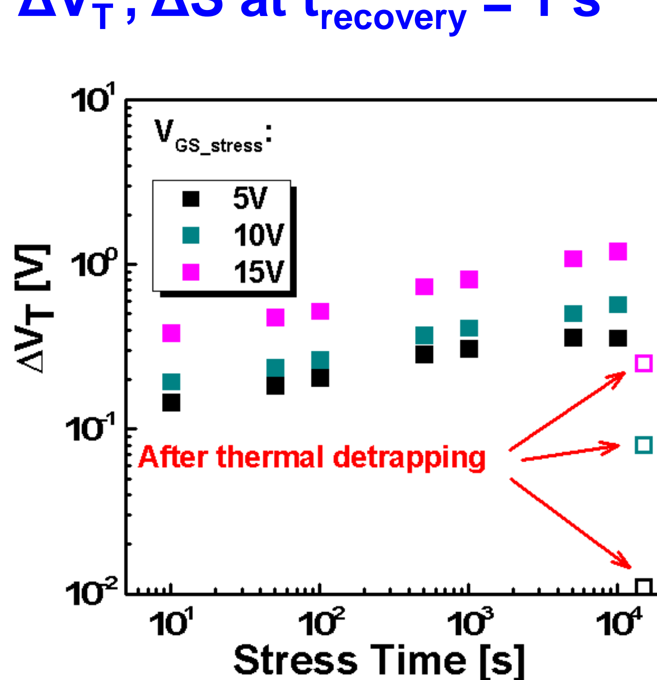
- First sample: ~ 1-2 s after removal of stress

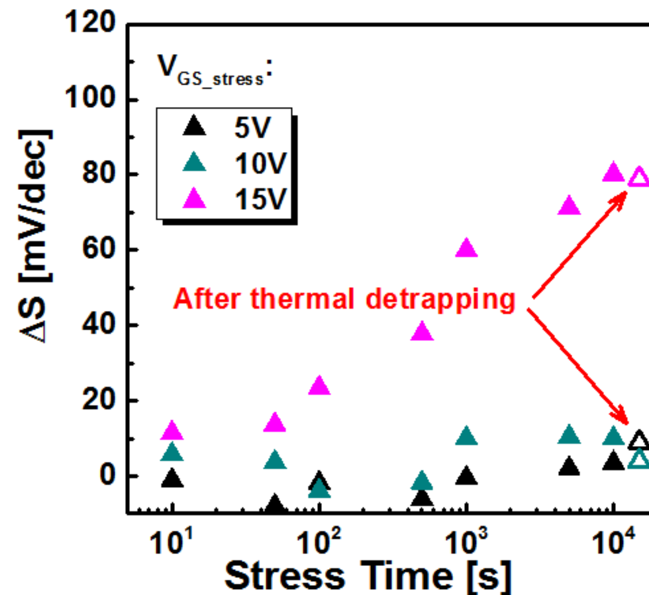
3. PBTI results

Voltage dependence of ΔV_T and ΔS at RT

- ΔV_T , ΔS at $t_{recovery}$ = 1 s

SiO$_2$





E field ~ 1, 2, 3 MV/cm

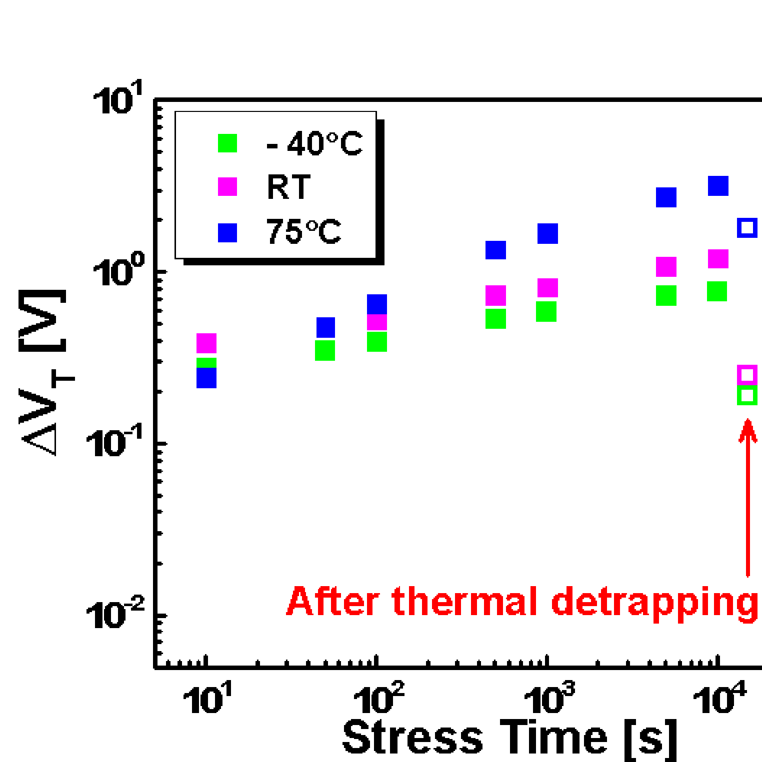
- t_{stress} ↑ → ΔV_T ↑
- V_{GS_stress} ↑ → ΔV_T ↑
- Minimal ΔS for 5 and 10 V stress, clear increase for 15 V stress
- After 15 V stress, partial V_T recovery, no S recovery

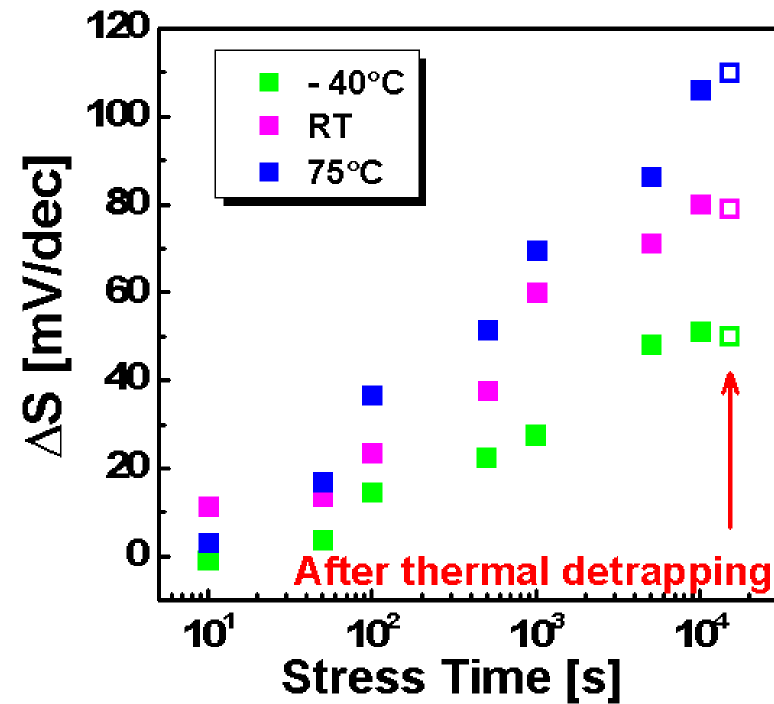
Temperature dependence of ΔV_T and ΔS

Stress conditions:

- V_{GS_Stress} = 15 V, T = -40°C, RT, 75°C, t_{stress}= 10 – 10,000 sec

SiO_2

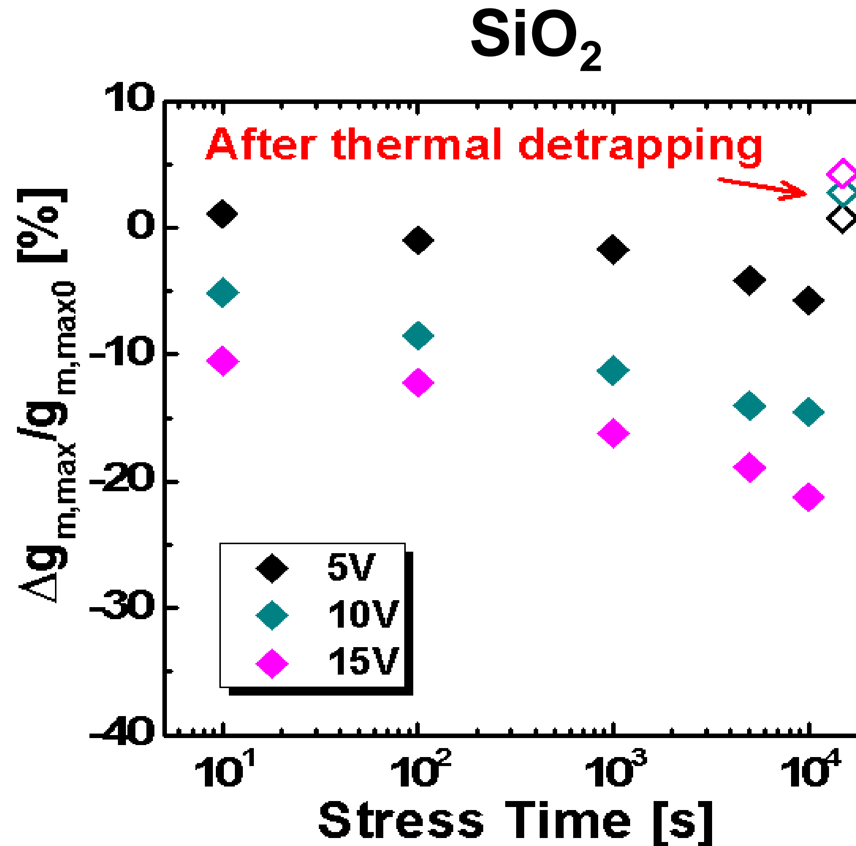




- T ↑ → ΔV_T ↑
- T ↑ → ΔS ↑
- Partial V_T recovery, no S recovery

Stress time and voltage evolution of $\Delta g_{m,max}$

- Different set of experiments, same stress conditions, RT



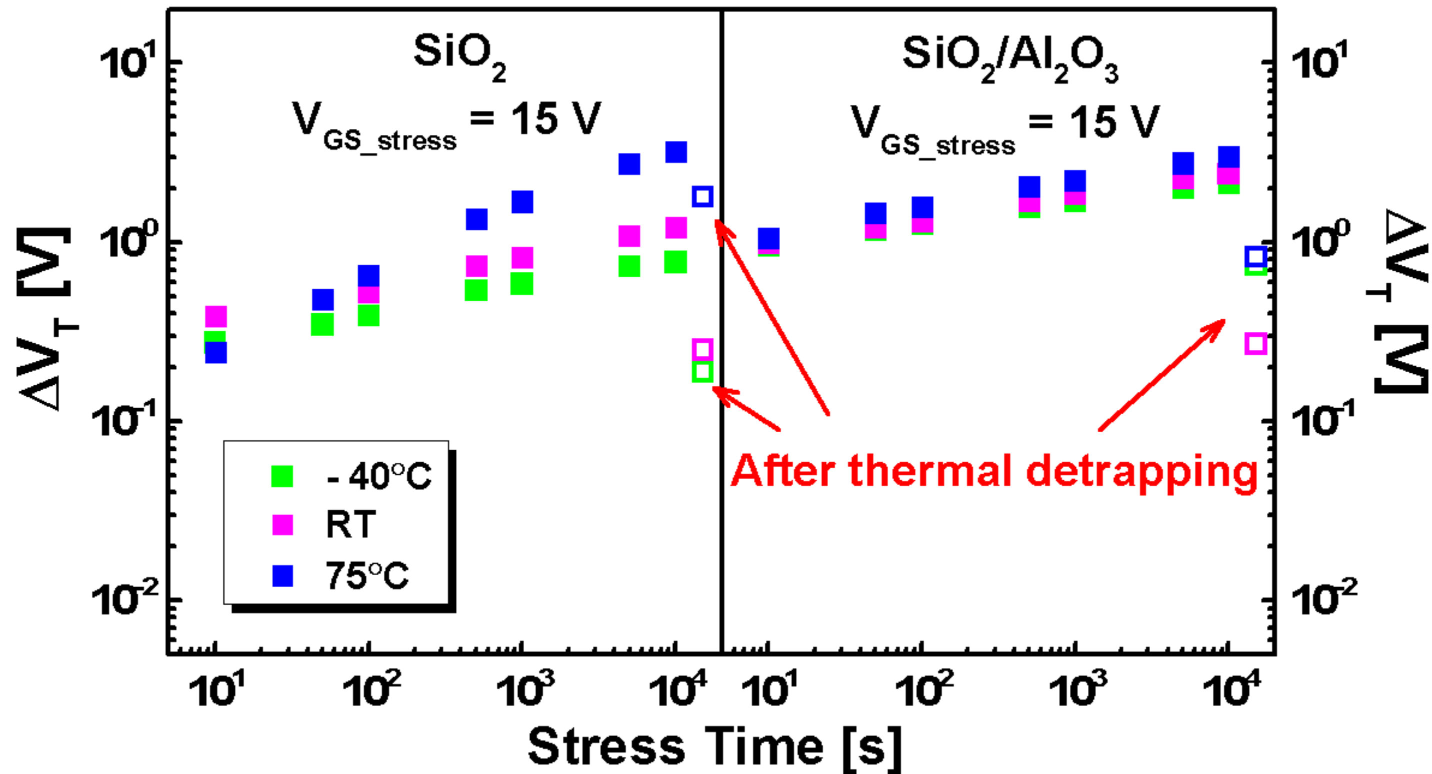
- t_{stress} ↑ → $|\Delta g_{m,max}|$ ↑
- V_{GS_stress} ↑ → $|\Delta g_{m,max}|$ ↑
- g_m completely recovers after thermal detrapping

SiO_2 devices summary

- **Positive ΔV_T increases with stress voltage, time and temperature**
- **ΔV_T recoverable under benign stress ($V_{GS_stress} \leq 10$ V, $T \leq RT$)**
- **ΔV_T partially recoverable under harsh stress**
- **ΔS non-recoverable under harsh stress**

SiO_2/Al_2O_3 vs. SiO_2 devices: ΔV_T

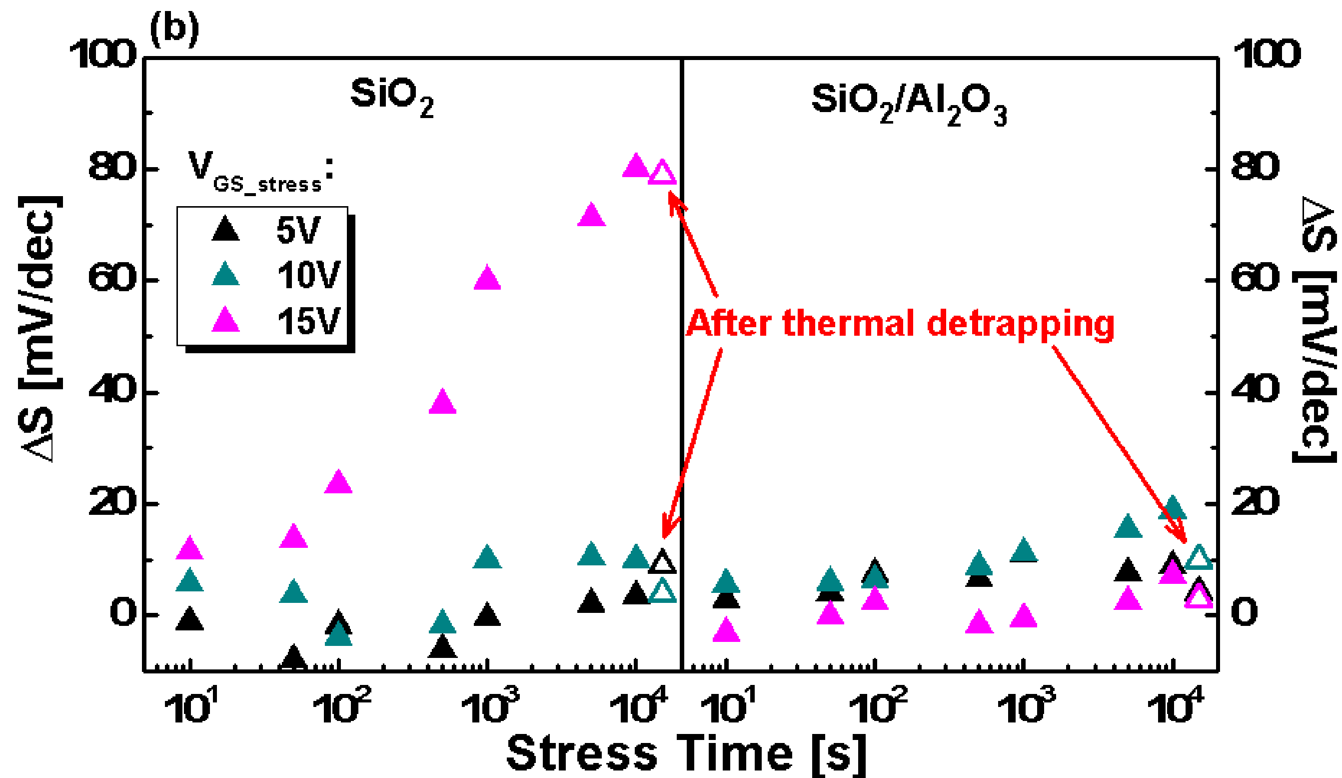
- ΔV_T at $t_{recovery}$ = 1s, T = -40°C, RT, 75°C, t_{Stress}= 10 – 10,000 sec



SiO_2/Al_2O_3 vs. SiO_2:
- Weaker T dependence
- Larger ΔV_T for T ≤ RT

SiO_2/Al_2O_3 vs. SiO_2 devices: ΔS

- ΔS at $t_{recovery}$ = 1s, RT

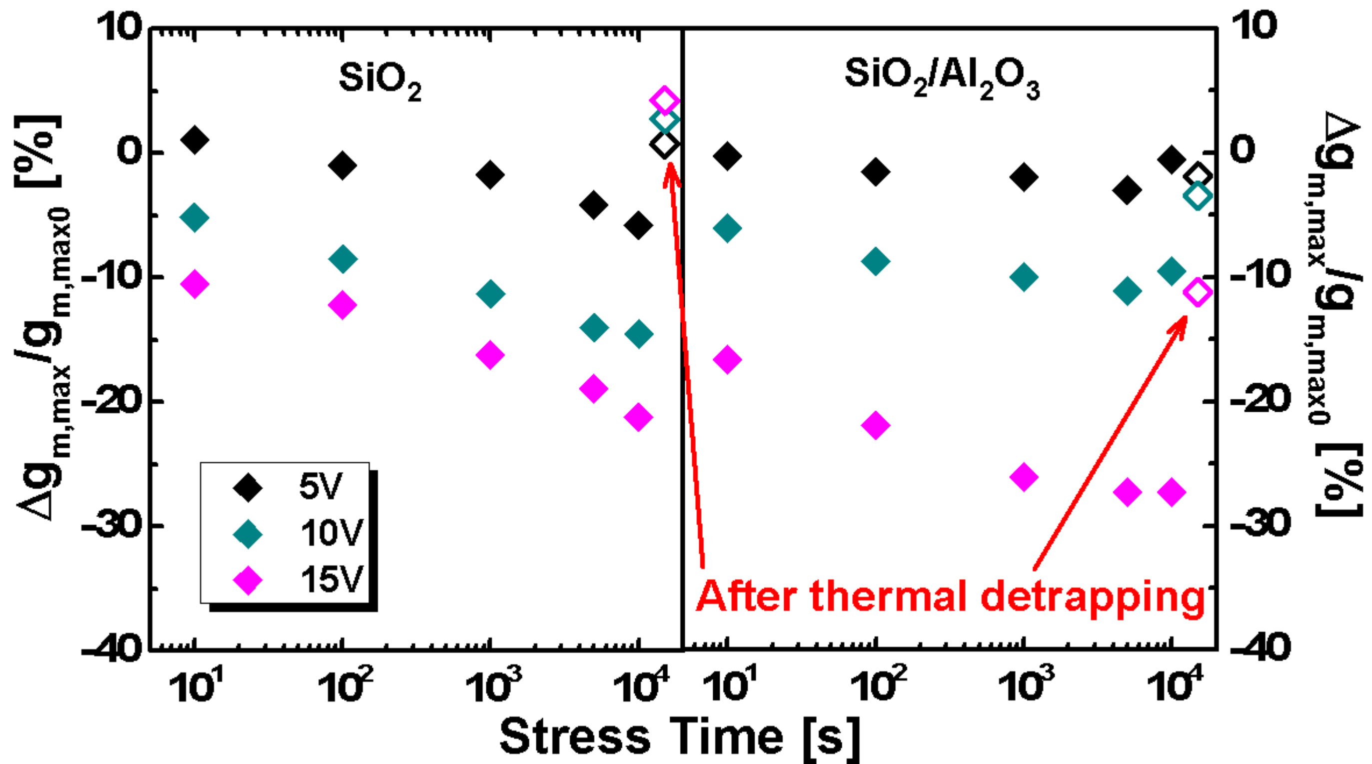


SiO_2/Al_2O_3 vs. SiO_2:

- Minimal ΔS for all stress voltages and T's

SiO_2/Al_2O_3 vs. SiO_2 devices: $\Delta g_{m,max}$

- $\Delta g_{m,max}$ after stress during ramp down, RT



SiO_2/Al_2O_3 vs. SiO_2:

- Partial recovery of g_m

SiO_2 devices vs. SiO_2/Al_2O_3 devices Summary

Similarities:

- Positive ΔV_T increases with stress voltage, time and temperature
- ΔV_T recoverable under benign stress
- ΔV_T partially recoverable under harsh stress

Differences:

- SiO_2/Al_2O_3 devices show larger ΔV_T at $T \leq RT$
- SiO_2/Al_2O_3 devices show weaker T dependence
- Both show non-recoverable ΔV_T under harsh stress, but
  - SiO_2 → shows non-recoverable ΔS
  - SiO_2/Al_2O_3 → shows non-recoverable $\Delta g_{m,max}$

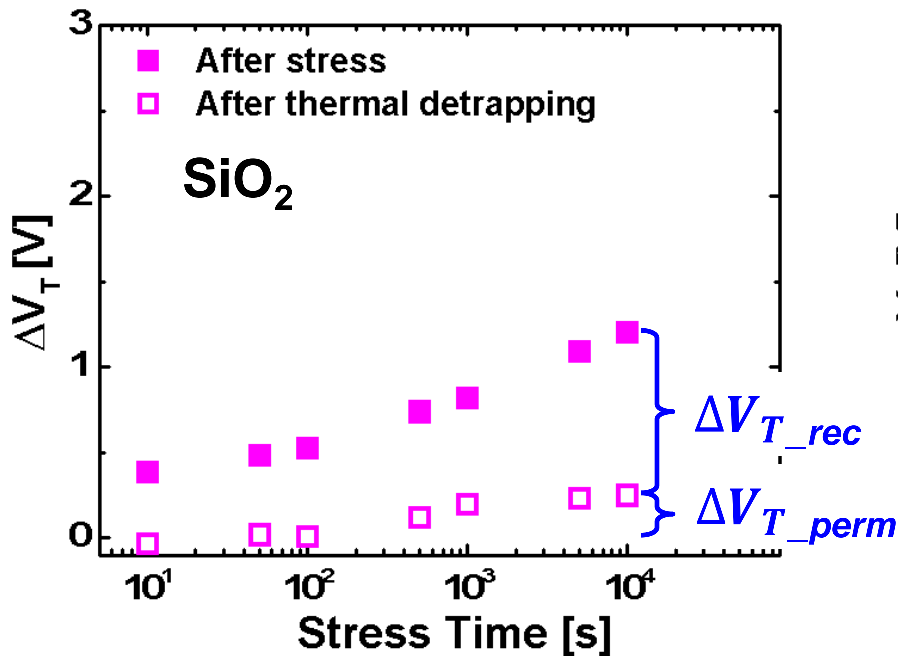
4. Discussion and modeling

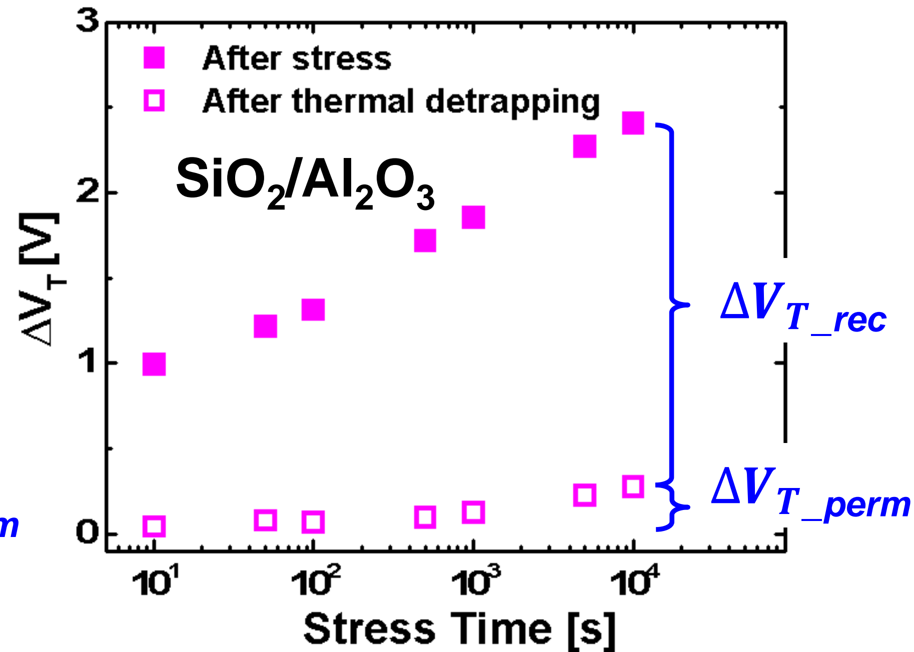
Mechanisms behind ΔV_T

For both dielectrics:

- **Recoverable ΔV_{T_rec} + Non-recoverable ΔV_{T_perm}**

V_{GS_stress} = 15 V at RT

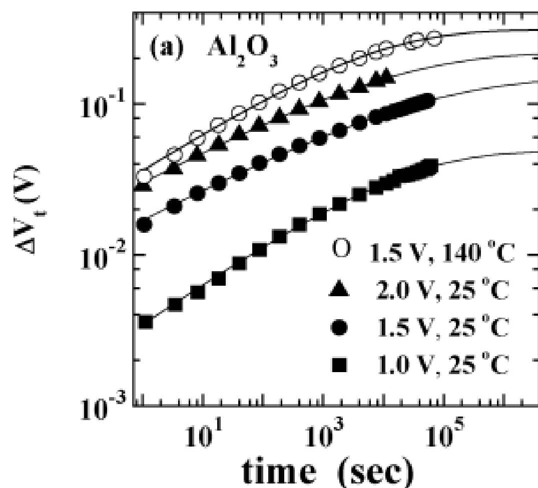




Recoverable ΔV_T under benign stress

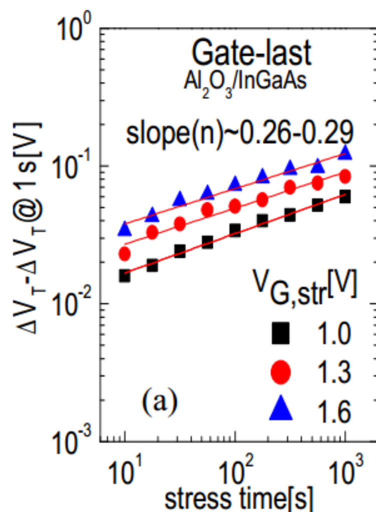
- $V_{GS_stress} \leq 10$ V, $T \leq$ RT
- Power law dependence with stress time
- Also observed in other MOS systems

Si

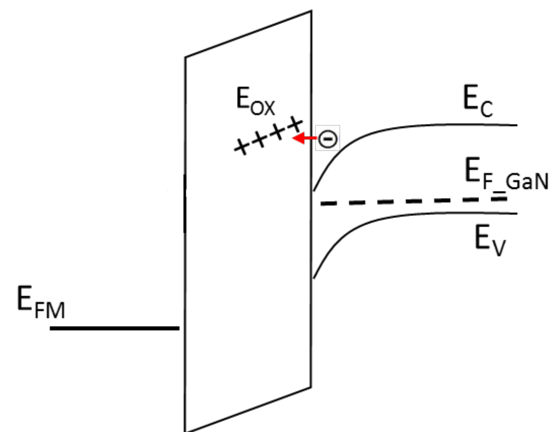


S. Zafar, TDMR 2005

InGaAs

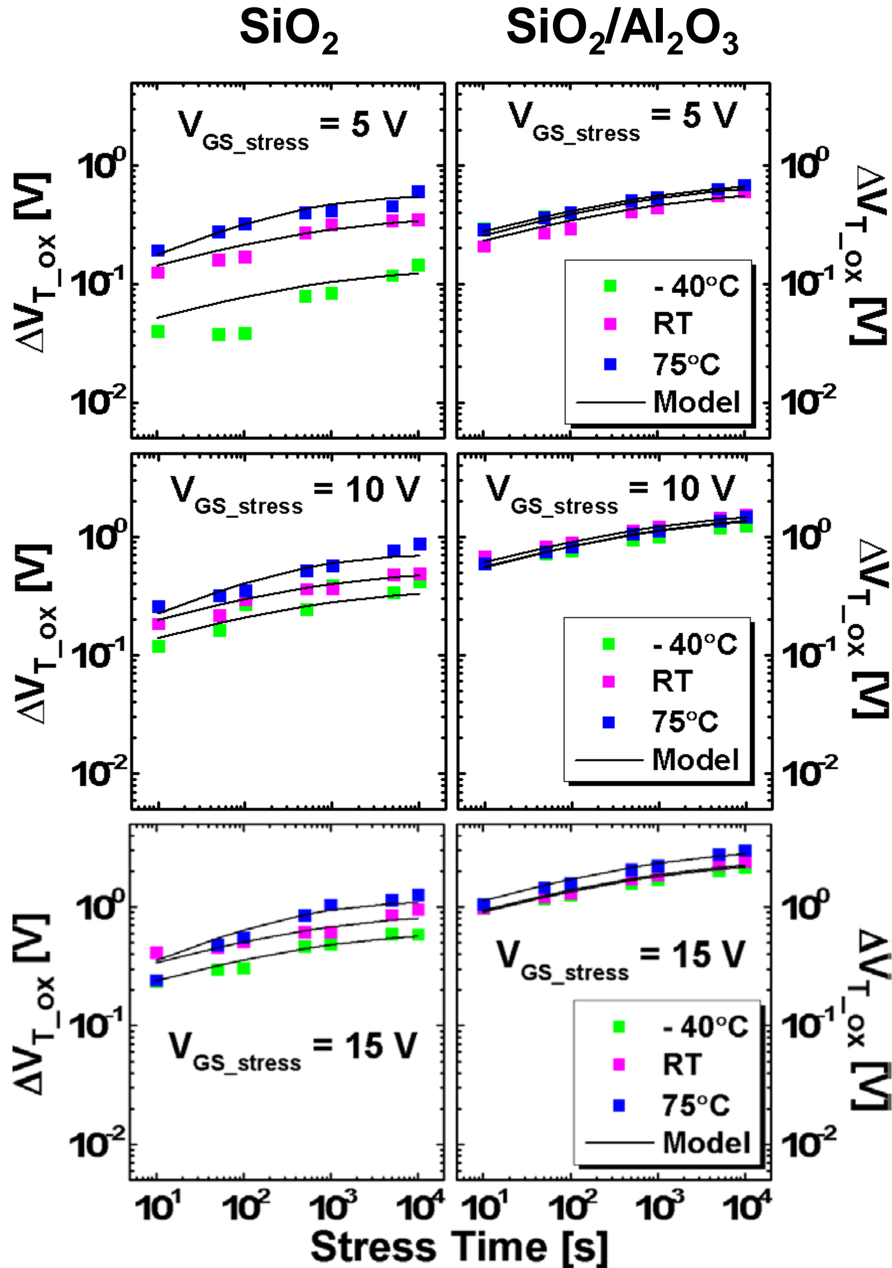


S. Deora, et al., IPRS 2014



- Consistent with electron trapping in pre-existing oxide traps

Oxide trapping model



$$\Delta V_{T_ox} = \Delta V_{max} \cdot \left\{1 - \exp\left(-\left(\frac{t}{\tau_0}\right)^{\beta}\right)\right\}$$

S. Zafar, TDMR 2005

- **t: stress time**
- **ΔV_{max} is function of trap density and trapped charge centroid**
- **β describes trap distribution**
- **τ_0 is time constant of traps**

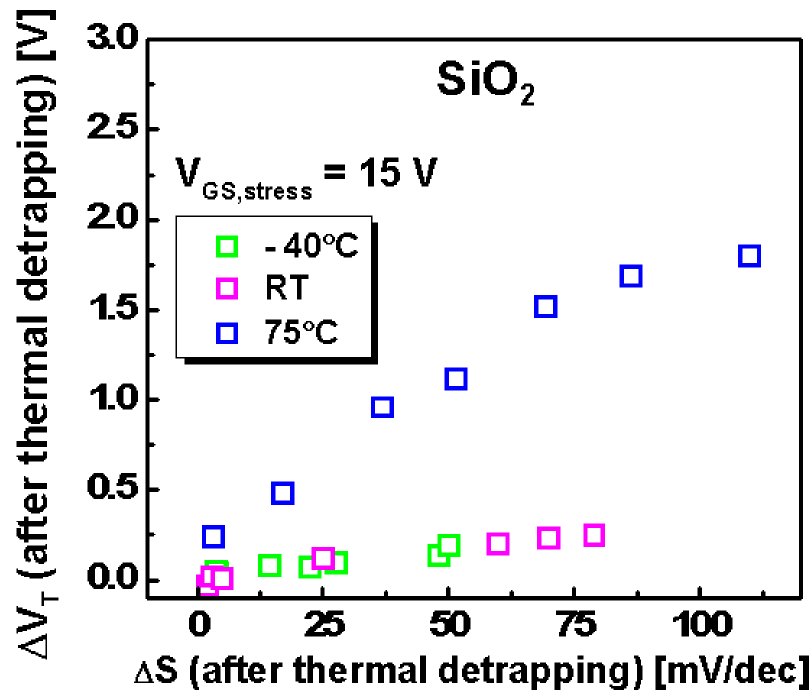
SiO_2: β = 0.25 ; τ_0= 150 s
SiO_2/Al_2O_3: β = 0.22-0.25 ; τ_0 = 200 s

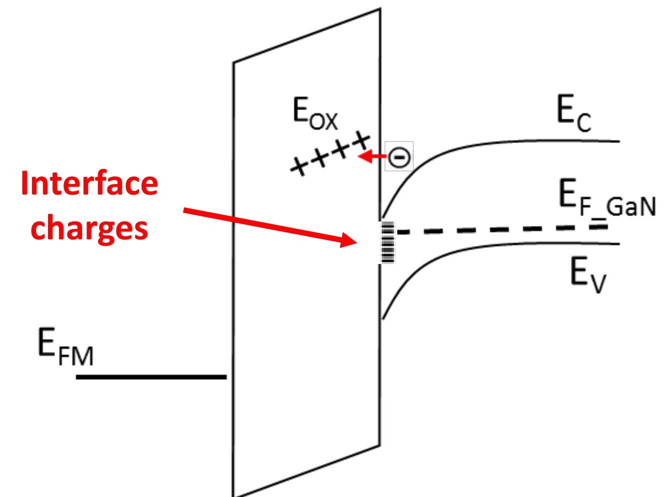
Channel	Oxide	β
Si	Al_2O_3	0.32
InGaAs	Al_2O_3, ZrO_2/Al_2O_3	0.26-0.29
GaN	SiO_2 , SiO_2/Al_2O_3	0.22-0.25

This work

Non-recoverable ΔV_T under harsher stress SiO_2 devices

- V_{GS_stress} = 15 V

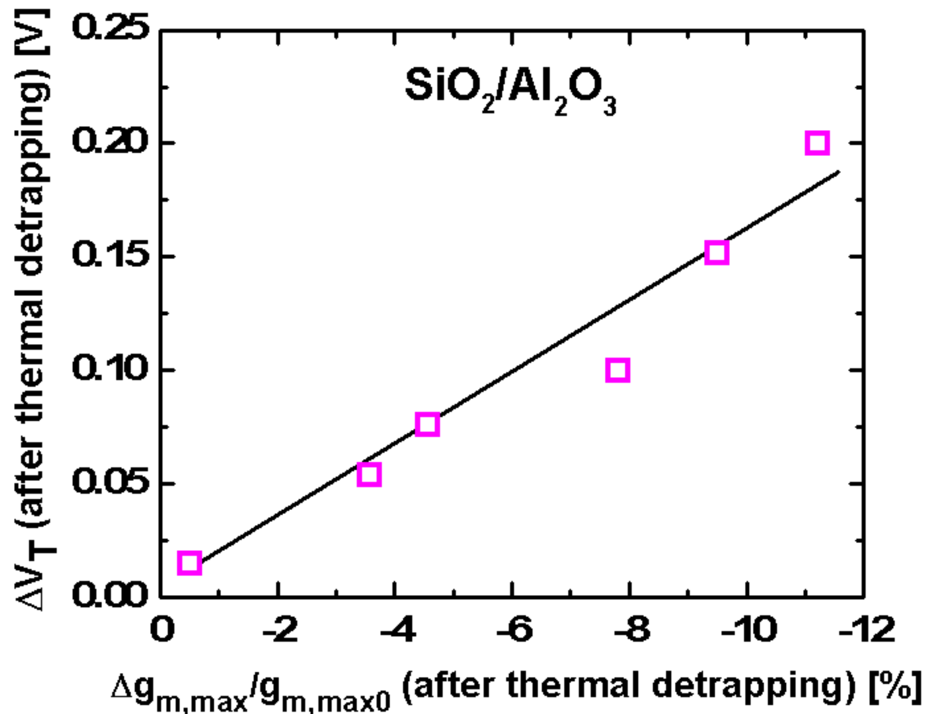


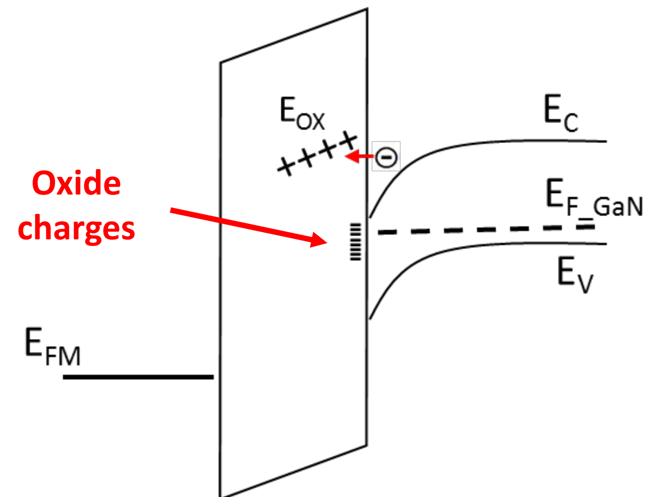


- Non-recoverable ΔV_T correlates with non-recoverable ΔS → generation of interface states

Non-recoverable ΔV_T under harsher stress SiO_2/Al_2O_3 devices

- V_{GS_stress} = 15 V, RT





- Non-recoverable ΔV_T correlates with non-recoverable $\Delta g_{m,max}$ → generation of oxide traps near Al_2O_3/GaN interface
- Also observed in Al_2O_3/InGaAs MOSFETs (*S. Deora, IRPS 2014*)

5. Conclusions

- **Under benign stress (V_{GS_stress} ≤ 10 V, T ≤ RT):**
  - **ΔV_T due to electron trapping in pre-existing oxide traps**
  - **ΔV_T mostly recoverable**

- **Under harsher stress (V_{GS_stress} = 15 V), additional non-recoverable ΔV_T:**
  - **SiO_2 → generation of interface states**
  - **SiO_2/Al_2O_3 → generation of oxide traps near oxide/GaN interface**

- **Oxide trapping model shows excellent agreement with experimental data at all T**

Questions?

Thank you